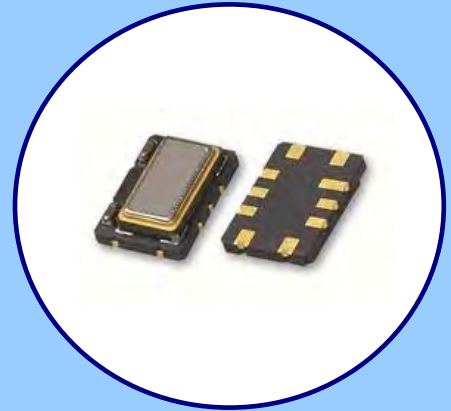


FEATURES

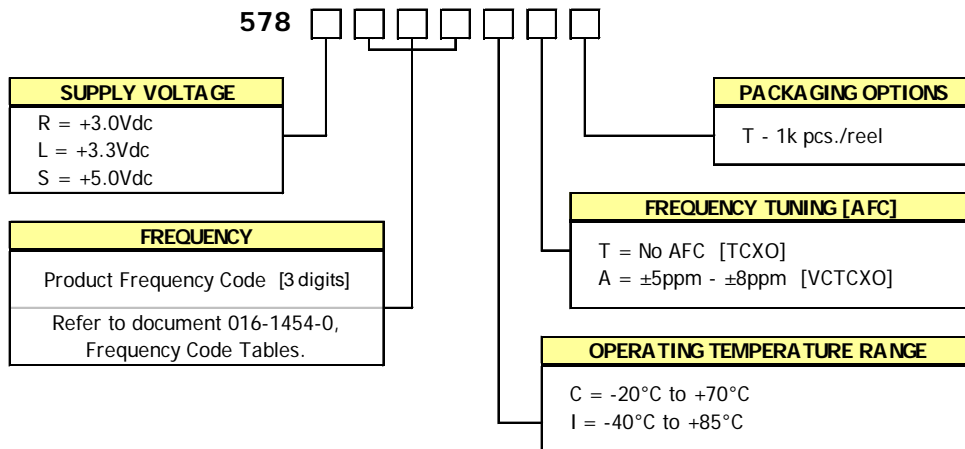
- **Clipped Sine Output**
- **Optional Voltage Control for Frequency Tuning [VCTCXO]**
- 7.0mmx5.0mm Surface Mount Package
- Frequency Range 5 – 52 MHz
- Fundamental Crystal Design
- Operating Voltage, +3.0Vdc, +3.3Vdc or +5.0Vdc
- Overall Frequency Stability ± 4.6 ppm
- Operating Temperature to -40°C to +85°C
- Tape & Reel Packaging Standard, EIA-418
- **RoHS/Green Compliant [6/6]**



APPLICATIONS

The Model 578, a quartz based analog TCXO with Clipped Sine output and optional frequency tuning, is suitable for applications requiring Stratum 3 performance such as base stations, Microcells, Femtocells, 1588 and Synchronous Ethernet timing, wireless communications, test and measurement.

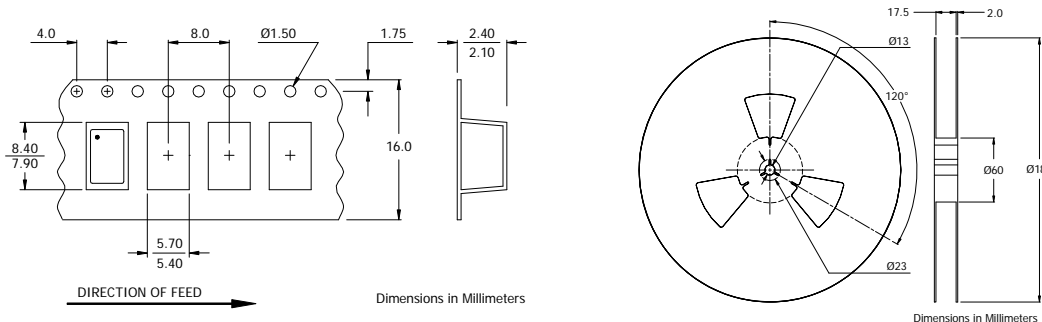
ORDERING INFORMATION



**Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.**

PACKAGING INFORMATION [reference]

Device quantity is 1k pcs. maximum per 180mm reel.

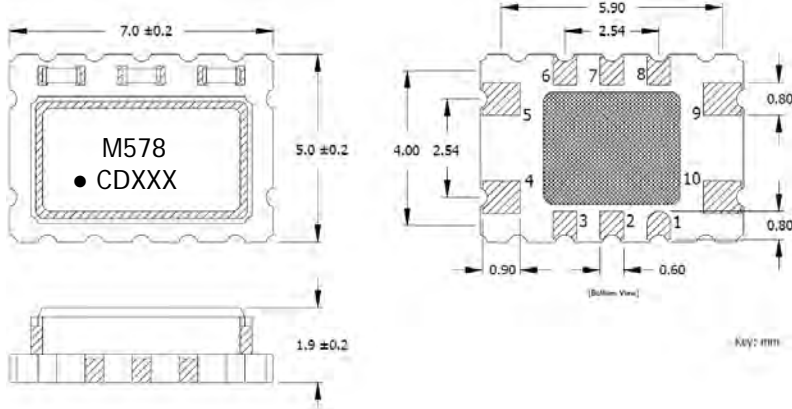


SHENZHEN YIJIN ELECTRONICS CO: LTD TEL: 0755-27876565

18924600166 QQ: 857950243 <http://www.vc-tcxo.com>

MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



MARKING INFORMATION

1. M578 – CTS Model Series.
 2. ● – Pin 1 identifier.
 3. C – CTS identifier.
 4. D – Date code. See Table II for codes.
 5. xxx – Frequency Code.
- Refer to document 016-1454-0, Frequency Code Tables.

NOTES

1. DO NOT make connections to non-labeled pins. Castellation pins may have internal connections used in the manufacturing process.
2. Termination pads (e4); barrier plating is nickel [Ni] with gold [Au] flash plate.
3. Reflow conditions per JEDEC J-STD-020, 260°C maximum.
4. MSL = 1.

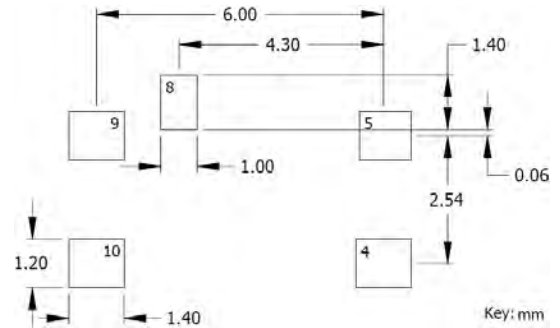
D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
4	GND	Circuit & Package Ground
5	Output	Clipped Sine Wave Output
8	EOH	Tri-State Enable
9	V _{CC}	Supply Voltage
10	V _C	Control Voltage – VCTCXO [Note 1] GND - TCXO

NOTES

1. Connect to ground for TCXO [no AFC] option.
2. DC-Cut Capacitor Required.
Add 1000pF capacitor between TCXO output and input of load.

SUGGESTED SOLDER PAD GEOMETRY



TEST CIRCUIT – CLIPPED SINE LOAD

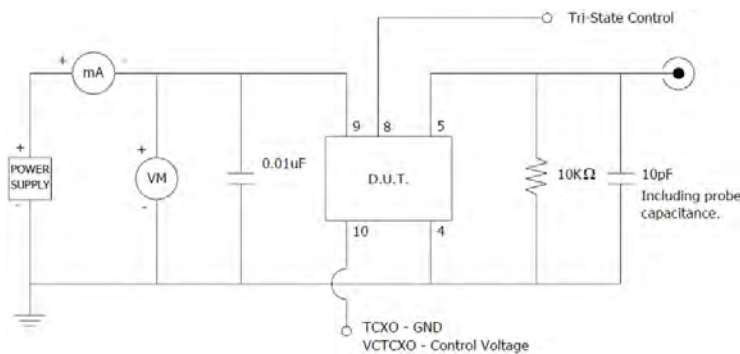


TABLE II – DATE CODE

YEAR		MONTH				JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
		2001	2005	2009	2013												
2001	2005	2009	2013	2017	A	B	C	D	E	F	G	H	J	K	L	M	
2002	2006	2010	2014	2018	N	P	Q	R	S	T	U	V	W	X	Y	Z	
2003	2007	2011	2015	2019	a	b	c	d	e	f	g	h	j	k	l	m	
2004	2008	2012	2016	2020	n	p	q	r	s	t	u	v	w	x	y	z	