

Features

- AEC-Q100 with extended temperature range (-55°C to 125°C)
- Frequencies between 1 MHz and 110 MHz accurate to 6 decimal places
- Supply voltage of 1.8V or 2.25V to 3.63V
- Excellent total frequency stability as low as ± 20 ppm
- Industry best G-sensitivity of 0.1 PPB/G
- Low power consumption of 3.8 mA typical at 1.8V
- LVCMOS/LVTTL compatible output
- Industry-standard packages: 2.0 x 1.6, 2.5 x 2.0, 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm x mm
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free

Applications

- Automotive, extreme temperature and other high-rel electronics
- Infotainment systems, collision detection devices, and in-vehicle networking
- Powertrain control



Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage.

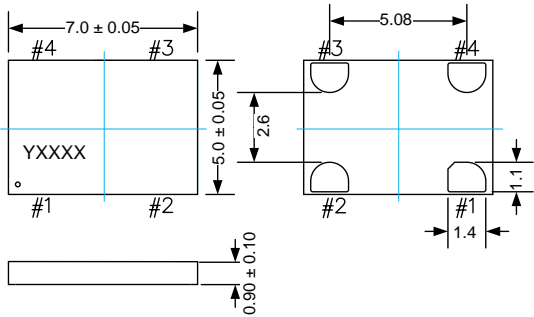
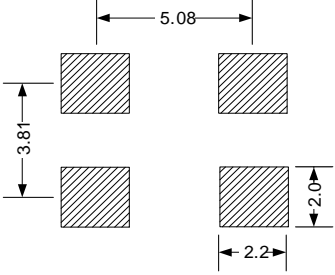
Table 1. Electrical Characteristics

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---------|------|------|------|------------|---|
| Frequency Range | | | | | | |
| Output Frequency Range | f | 1 | – | 110 | MHz | Refer to Table 13 and Table 14 for a list supported frequencies |
| Frequency Stability and Aging | | | | | | |
| Frequency Stability | F_stab | -20 | – | +20 | ppm | Inclusive of Initial tolerance at 25°C, 1st year aging at 25°C, and variations over operating temperature, rated power supply voltage and load (15 pF \pm 10%). |
| | | -25 | – | +25 | ppm | |
| | | -30 | – | +30 | ppm | |
| | | -50 | – | +50 | ppm | |
| Operating Temperature Range | | | | | | |
| Operating Temperature Range (ambient) | T_use | -40 | – | +85 | °C | Industrial, AEC-Q100 Grade3 |
| | | -40 | – | +105 | °C | Extended Industrial, AEC-Q100 Grade2 |
| | | -40 | – | +125 | °C | Automotive, AEC-Q100 Grade 1 |
| | | -55 | – | +125 | °C | Extended Temperature, AEC-Q100 |
| Supply Voltage and Current Consumption | | | | | | |
| Supply Voltage | Vdd | 1.62 | 1.8 | 1.98 | V | All voltages between 2.25V and 3.63V including 2.5V, 2.8V, 3.0V and 3.3V are supported. |
| | | 2.25 | – | 3.63 | V | |
| Current Consumption | Idd | – | 4.0 | 4.8 | mA | No load condition, f = 20 MHz, Vdd = 2.25V to 3.63V |
| | | – | 3.8 | 4.5 | mA | No load condition, f = 20 MHz, Vdd = 1.8V |
| LVCMOS Output Characteristics | | | | | | |
| Duty Cycle | DC | 45 | – | 55 | % | All Vdds |
| Rise/Fall Time | Tr, Tf | – | 1.5 | 3 | ns | Vdd = 2.25V - 3.63V, 20% - 80% |
| | | – | 1.3 | 2.5 | ns | Vdd = 1.8V, 20% - 80% |
| Output High Voltage | VOH | 90% | – | – | Vdd | IOH = -4 mA (Vdd = 3.0V or 3.3V) IOH = -3 mA (Vdd = 2.8V and Vdd = 2.5V) IOH = -2 mA (Vdd = 1.8V) |
| Output Low Voltage | VOL | – | – | 10% | Vdd | IOL = 4 mA (Vdd = 3.0V or 3.3V) IOL = 3 mA (Vdd = 2.8V and Vdd = 2.5V) IOL = 2 mA (Vdd = 1.8V) |
| Input Characteristics | | | | | | |
| Input High Voltage | VIH | 70% | – | – | Vdd | Pin 1, OE |
| Input Low Voltage | VIL | – | – | 30% | Vdd | Pin 1, OE |
| Input Pull-up Impedence | Z_in | – | 100 | – | k Ω | Pin 1, OE logic high or logic low |
| Startup and Resume Timing | | | | | | |
| Startup Time | T_start | – | – | 10 | ms | Measured from the time Vdd reaches its rated minimum value |
| Enable/Disable Time | T_oe | – | – | 130 | ns | f = 110 MHz. For other frequencies, T_oe = 100 ns + 3 * cycles |
| Jitter | | | | | | |
| RMS Period Jitter | T_jitt | – | 1.6 | 2.5 | ps | f = 75 MHz, 2.25V to 3.63V |
| | | – | 1.9 | 3.0 | ps | f = 75 MHz, 1.8V |
| RMS Phase Jitter (random) | T_phj | – | 0.5 | – | ps | f = 75 MHz, Integration bandwidth = 900 kHz to 7.5 MHz |
| | | – | 1.3 | – | ps | f = 75 MHz, Integration bandwidth = 12 kHz to 20 MHz |

Dimensions and Patterns

| Package Size – Dimensions (Unit: mm) ^[10] | Recommended Land Pattern (Unit: mm) ^[11] |
|--|---|
| <p>2.0 x 1.6 x 0.75 mm</p> | |
| <p>2.5 x 2.0 x 0.75 mm</p> | |
| <p>3.2 x 2.5 x 0.75 mm</p> | |
| <p>5.0 x 3.2 x 0.75 mm</p> | |

Dimensions and Patterns

| Package Size – Dimensions (Unit: mm) ^[10] | Recommended Land Pattern (Unit: mm) ^[11] |
|--|--|
| <p>7.0 x 5.0 x 0.90 mm</p>  |  |

Notes:

10. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
11. A capacitor of value 0.1 μ F or higher between Vdd and GND is required.